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ASIC BIST synthesis: a VHDL approach

Eberle, T. McVay, B. Meyers, C. Moore, J.
DFT Technol. Group, Sanders Associates Inc., Nashua, I USA;

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Abstract:
This paper describes the practical aspects of an automa design process and tool environment developed to rapic effectively include **BIST** into ASIC designs. An overview **BIST** architecture is given describing **BIST** capabilities mission logic, embedded and external **memory**, device an interconnect **BIST** capability used to assist module/I **BIST**. A high level synthesis approach is employed usin VHDL language in a way unique to its intended purpose automatic means for **instantiating** VHDL **BIST** structu

an ASIC design is described. Other automated phases c development cycle are discussed including testability enhancement of the ASIC core and test stimulus genera foundry, factory, and field test. Results are presented f ASIC designs ranging in gate count from 56 k-164 k ga (complexity from controllers to data processors)

Index Terms:

SRAM chips application specific integrated circuits automatic equipment automatic testing built-in self test design for testa hardware description languages high level synthesis logic tes production testing 56 to 164 k ASIC **BIST** synthesis ASIC d ASIC mission logic **BIST** architecture SRAM VHDL languag automated design controllers data processors embedded m external **memory** factory testing field test foundry high lev synthesis interconnect **BIST** module/PCB **BIST** test stimulu generation

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